WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

a semiconductor chip provided with an integrated circuit and a pad that is electrically connected to the integrated circuit;

a wiring layer that has a concave portion and is electrically connected to the pad;

an external terminal that is joined to the concave portion of the wiring layer; and

a resin layer provided with a through hole and disposed on the wiring layer, the through hole and the concave portion residing at the same position.

2. The semiconductor device according to claim 1, wherein a width of the concave portion increases with a depth of the concave portion.

3. The semiconductor device according to claim 1, wherein the concave portion has a first width at a first depth and a second width at a second depth that is deeper than the first depth, the first width being larger than an opening size of the concave portion and the second width being smaller than the first width.

4. The semiconductor device according to claim 1, wherein an inner surface of the through hole in the resin layer is in contact with the external terminal.

5. The semiconductor device according to claim 1, further comprising a

stress relaxation layer disposed on the semiconductor chip, wherein the wiring layer is disposed on the stress relaxation layer.

6. The semiconductor device according to claim 1, wherein the resin layer is prepared from a solder resist.

7. A circuit board comprising a semiconductor device according to claim 1.

8. An electronic apparatus comprising a semiconductor device according to claim 1.

9. A semiconductor wafer, comprising:

a semiconductor substrate provided with a plurality of integrated circuits and pads with each pad electrically connected to each of the integrated circuits;

a wiring layer that has a concave portion and is electrically connected to the pads;

an external terminal that is joined to the concave portion of the wiring layer; and

a resin layer provided with a through hole and disposed on the wiring layer, the through hole and the concave portion residing at a same position.

10. The semiconductor wafer according to claim 9, wherein a width of the concave portion increases a depth of the concave portion.

11. The semiconductor wafer according to claim 9, wherein the concave

portion has a first width at a first depth and a second width at a second depth that is deeper than the first depth, the first width being larger than an opening size of the concave portion and the second width being smaller than the first width.

12. The semiconductor wafer according to claim 9, wherein an inner surface of the through hole in the resin layer is in contact with the external terminal.

13. The semiconductor wafer according to claim 9, further comprising a stress relaxation layer disposed on the semiconductor substrate, wherein the wiring layer is disposed on the stress relaxation layer.

14. The semiconductor wafer according to claim 9, wherein the resin layer is prepared from a solder resist.

15. A method for manufacturing a semiconductor device, comprising:

forming a wiring layer over a semiconductor substrate provided with a integrated circuit and a pad that is electrically connected to the integrated circuit;

electrically connecting the wiring layer to the pad;

forming a resin layer so as to cover the wiring layer;

forming a through hole and a concave portion in the resin layer and the wiring layer respectively, the through hole and the concave portion residing at a same position; and

providing an external terminal joining the concave portion of the wiring

layer.

16. The method for manufacturing a semiconductor device according to claim 15, further comprising forming the through hole in the resin layer and then forming the concave portion in the wiring layer.

17. The method for manufacturing a semiconductor device according to claim 15, further comprising increasing a width of the concave portion with a depth of the concave portion.

18. The method for manufacturing a semiconductor device according to claim 15, further comprising placing an inner surface of the through hole in the resin layer in contact with the external terminal.

19. The method for manufacturing a semiconductor device according to claim 15, further comprising disposing a stress relaxation layer on the semiconductor substrate, wherein the wiring layer is disposed on the stress relaxation layer.

20. The method for manufacturing a semiconductor device according to claim 15, further comprising forming the resin layer from a solder resist.